

# A Low-Phase-Noise 5GHz Quadrature CMOS VCO using Common-Mode Inductive Coupling

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## Abstract

*A new concept for quadrature coupling of LC oscillators is introduced and demonstrated on a 5GHz CMOS VCO. It uses injection-locking through common-mode inductive coupling to enforce quadrature. The technique provides quadrature over a wide tuning range without introducing any phase noise- or power consumption increase. The realized VCO is tunable between 4.6GHz and 5.2GHz and measures a phase noise lower than  $-124\text{dBc/Hz}$  at 1MHz offset over the entire tuning range. The circuit draws 8.75mA from a 2.5V supply.*

## 1. Introduction

The wireless LAN market is expected to continue its exponential growth in the coming years. In this market, the 5GHz 54Mb/s 802.11a standard is slowly replacing the 2.4GHz 11Mb/s 802.11b standard. The development of single-chip 802.11a CMOS solutions is desirable to enable implementations at lowest cost. The full integration of transceivers implies the use of low-IF or zero-IF architectures that require quadrature signals for I/Q-(de)modulation.

Several techniques exist to generate quadrature. A VCO running at the double frequency can be divided by two to give quadrature. This solution shows poor quadrature accuracy, as it requires an accurate 50% duty cycle VCO. A VCO followed by a polyphase filter gives quadrature [1]; however, it requires buffers that increase the power consumption considerably. Alternatively, two separate oscillators can be forced to run in quadrature by using coupling transistors [2]. This approach suffers from a trade-off between accurate quadrature and low phase noise. Moreover, the coupling transistors increase the power consumption. To circumvent the phase noise penalty, additional  $90^\circ$  phase shifters can be placed at the gates of the coupling transistors [3-5]. However, the increase in power consumption remains. Recently, an alternative quadrature topology has been proposed, where the negative resistance transistors are cascoded by the coupling transistors [6]. Although this approach gives

low phase noise and does not increase power consumption, the technique is not well suited for implementation of widely tunable oscillators in the 5GHz range. This is because the coupling transistors have to be about five times larger than the negative resistance transistors [6], thus loading the oscillator with large parasitic capacitors that limit the tuning range.

The solutions so far proposed suffer from an increase in phase noise and/or an increase in power consumption or they result in a limited tuning range, when used at high frequencies of oscillation.

This paper presents a fully integrated 5GHz quadrature CMOS VCO that uses a new technique to generate quadrature over a wide tuning range without suffering from an increase in power consumption and phase noise. The technique uses injection-locking through common-mode inductive coupling to enforce the quadrature relation between two oscillators. The proposed oscillator is implemented in a 0.25- $\mu\text{m}$  CMOS process.

## 2. Quadrature by common mode coupling

The schematic view of the proposed quadrature oscillator is shown in Figure 1. It consists of two separate oscillators whose common-mode  $2^{\text{nd}}$ -order harmonics are coupled by the inductor pair  $L_5, L_6$ .

The quadrature behavior can be explained by first focussing on the waveforms occurring in one of the two oscillators, shown in Figure 2. Due to the varactors, the two single-ended output waveforms are distorted. The varactors are accumulation-depletion pMOS devices: they exhibit a step-like  $C(V)$  curve with maximum capacitance at high gate-to-well voltages. Therefore, when the single-ended waveform voltage is high, the associated varactor capacitance is high and the waveform "slows down" and flattens. When the voltage is low, the capacitance is low and the waveform "speeds up" and sharpens. This gives rise to a  $2^{\text{nd}}$  order harmonic that shows up as a common-mode signal. The minima of the  $2^{\text{nd}}$  order harmonic align in phase with the minima of the fundamental [7].

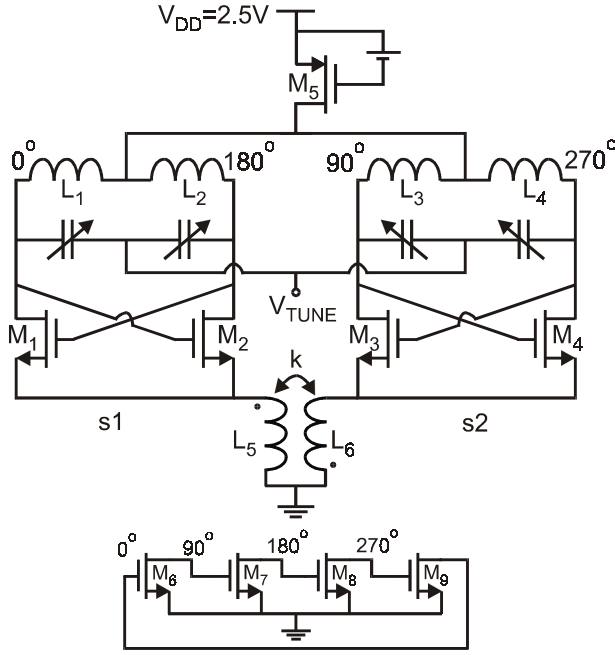


Figure 1. Schematic of the quadrature VCO.

The inductors  $L_1$  and  $L_2$  in Figure 1 are deliberately not combined into a single symmetrical inductor (the same holds for  $L_3, L_4$ ) but rather each inductor is implemented separately. A symmetrical inductor exhibits a larger quality factor when driven differentially [8]. This would result in a larger suppression of the common mode 2<sup>nd</sup> harmonic, which is instead necessary to maximize quadrature coupling in this topology.

Being a common mode signal, the 2<sup>nd</sup>-order harmonic does not appear at the differential output of the two separate oscillators. However, it is present in the common-mode current flowing through transistors  $M_{1..4}$ . By anti-phase coupling the common-mode currents of the two oscillators, the respective output waveforms at frequency  $f_0$  are forced to run in quadrature. This anti-phase coupling is implemented by means of the coupled inductors  $L_5$  and  $L_6$ . Figure 2 shows the four simulated quadrature output waveforms, along with the source voltages  $V_{S1}$  and  $V_{S2}$ .

In order to maximize the oscillation amplitude, the minima of  $V_{S1}$  and  $V_{S2}$  need to align with the minima of the output waveforms, as depicted in Figure 2. This condition is satisfied if the impedance at the sources is real at frequency  $2f_{osc}$ . Therefore, the tail inductor value is chosen to give resonance at  $2f_{osc}$ .

Figure 2 also shows that both  $V_{GS}$  and  $V_{DS}$  of transistors  $M_{1..4}$  become nearly zero during portions of the oscillation period. Thus,  $M_{1..4}$  are periodically pushed into deep triode at the waveform minima and they can conduct current only close to the zero crossings of the waveforms. Since the current pulses of  $M_1$  and  $M_2$  (and of  $M_{3,4}$ ) are 180° out of phase, their sum runs at  $2f_{osc}$ . Its maxima align with the zero-crossings of the fundamental and thus it is in phase with the 2<sup>nd</sup> harmonic coming from

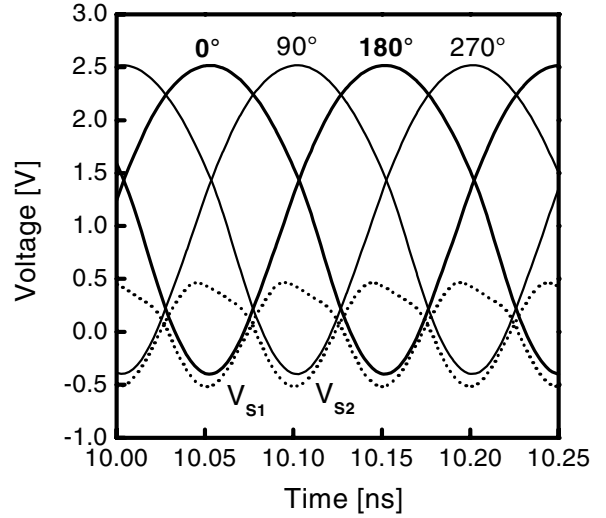


Figure 2. Simulated waveforms of the VCO.

the varactors. This provides an additional contribution to the 2<sup>nd</sup> harmonic that helps to maintain a strong quadrature coupling.

Transistors  $M_{6,9}$  in Figure 1 are minimum-size devices that are added to give directivity to the quadrature phases. Without them, the oscillator would have no preference for either +90° or -90° phase difference. The current flowing through  $M_{6,9}$  is negligible compared to the current in the transistors  $M_{1..4}$ , as the ratio in their  $(W/L)$ 's is more than one hundred.

### 3. Ring-based quadrature coupling versus injection-locked coupling

In the following, we compare the fundamental differences between ring-based quadrature VCO's and the new coupling scheme based on injection locking.

In quadrature LC oscillators based on a ring structure, the frequency of oscillation is not necessarily coincident with the resonance frequency of the individual tanks. The Barkhausen criterion applied to a conventional four-stage ring oscillator implies that the phase shift across each stage of the ring is 90°. However, the maximum phase shift between voltage and current that a resonator can provide is  $\pm 90^\circ$ ; this condition only occurs at frequencies where the impedance drops to zero and the phase diagram is flat. Therefore, phase shifters must be included in the loop.

In the two-stage quadrature oscillator topology proposed in [2], a 45° phase shift per stage is obtained by summing two quadrature signals. Another 180° phase shift is obtained by a simple sign-inversion. As a result, the oscillation frequency is forced to deviate from the tank resonance frequency, enabling each resonator to

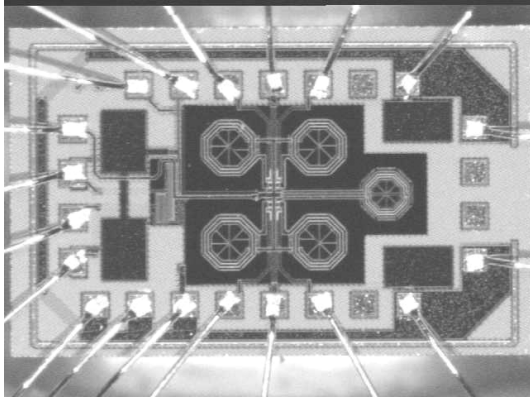


Figure 3. Chip photograph.

provide  $45^\circ$  of phase shift. However, the tank is now no longer operating at the frequency where the impedance is maximum and the phase characteristic is steepest. Consequently, the oscillation amplitude and the phase stability are reduced and the phase noise increases.

This problem has been addressed in [3,4,5] by applying additional phase shift, such that the tanks operate at zero phase shift, i.e. at their resonance frequency. However, the additional phase shifters increase power consumption and design complexity, and can potentially introduce extra noise.

In the proposed VCO, two oscillators are coupled through reciprocal injection locking. This mechanism only enforces the quadrature phase relation between the two oscillators and does not require the oscillation frequency to deviate from the tank resonance. Consequently, the coupling does not reduce the phase stability of each individual oscillator and no phase noise increase is seen. Moreover, since the quadrature coupling is established by means of coupled inductors rather than by transistors, the coupling devices introduce no significant extra sources of noise.

The coupling inductors  $L_5$  and  $L_6$  have additional beneficial effects on phase noise whilst not increasing the power consumption. They allow the oscillation waveforms to reach values below the negative supply rail (see Figure 2). Thus, the oscillation amplitude is maximized and the  $1/f^2$ -phase noise is reduced. In addition, the coupling inductors enable the  $V_{GS}$  and  $V_{DS}$  of  $M_{1,4}$  to periodically reach zero-value. This helps to reduce their contribution to  $1/f^3$ -phase noise [9].

Injection locking techniques are often considered not enough reliable. They feature a limited capture range that is difficult to predict in practical cases. However, here, a sufficient capture range is only required to overcome potential mismatches between the two tanks.

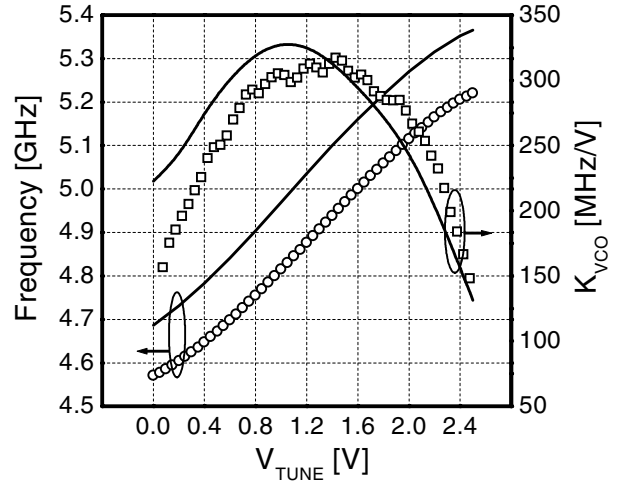


Figure 4. Simulated (solid) and measured (dots) tuning curves and their derivatives.

#### 4. Implementation

The proposed quadrature VCO is realized in Agere Systems' 0.25- $\mu\text{m}$  CMOS process. The inductors are laid out in the three top metal layers of this five Al-metal layer process. An in-house electro-magnetic simulator (IES<sup>3</sup>) is used to model all inductors.

Figure 3 shows a photograph of the chip. The four inductors  $L_{1,4}$  of the oscillator core are in the center of the figure. They have a simulated inductance of 1.8nH and a quality factor of 9 at 5GHz. The coupled inductors  $L_{5,6}$  are laid out as a center tapped symmetrical inductor (see right hand side of Figure 3). This inductor is intentionally placed relatively further from the core, to minimize parasitic coupling to the other inductors. Its connecting leads are also included in the electro-magnetic simulation. The two coupled inductors have a simulated inductance of 0.62nH each and a coupling coefficient  $k$  of 0.55 at 10GHz.

The layout is highly symmetrical, not only with respect to the signal paths, but also with respect to the ground return paths. All ground currents combine in one point in the center of the oscillator layout and go from there through a single path to the ground bondpads. The supply is de-coupled by means of on-chip capacitors.

#### 5. Experimental Results

The simulated and measured tuning curves are shown in Figure 4. The shapes of the two curves are nearly identical. The measured tuning curve is only offset by about 100MHz with respect to the simulated one. This is most likely due to inaccuracies in the estimated stray capacitances. The oscillator is tunable between 4.57 and 5.21GHz (13% tuning range). The maximum and minimum values of  $K_{VCO}$  are within a  $\pm 35\%$  range of the average value of 233MHz/V. The relatively constant  $K_{VCO}$  is due to the large signal amplitude, which effectively averages the steep  $C(V)$ -curve of the varactor

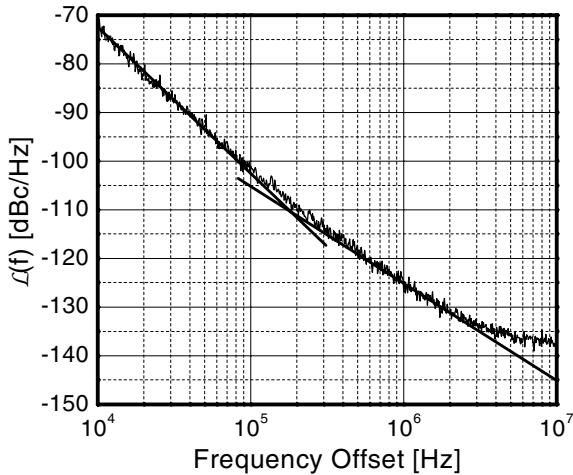


Figure 5. Measured phase noise at  $f_{osc}=4.88\text{GHz}$ .

[7]. A constant  $K_{VCO}$  is beneficial for PLL design, since it gives a constant loop gain and thus does not require dynamic adjustment of the charge pump current.

Figure 5 shows the phase noise at  $f_{osc}=4.88\text{GHz}$ . It measures  $-125\text{dBc/Hz}$  at  $1\text{MHz}$  offset from the carrier. At offset frequencies larger than about  $2\text{MHz}$ , the measured phase noise is limited to  $-140\text{dBc/Hz}$  by the noise floor of the measurement setup.

Figure 6 shows the measured phase noise along the entire tuning range, for offset frequencies of  $10\text{kHz}$  (flicker-noise dominated) and  $1\text{MHz}$  (white-noise dominated). Both the  $1/f^3$ - and  $1/f^2$ -phase noise are remarkably constant over the tuning range. The worst-case noise levels are  $-71\text{dBc/Hz}$  at  $10\text{kHz}$  and  $-124.5\text{dBc/Hz}$  at  $1\text{MHz}$ . Table 1 shows a comparison of the achieved figure of merit (FOM) [10] to that of other published quadrature oscillators. All FOMs are calculated from the worst-case phase noise.

Table 1. Comparison with previous art

Ref.	$f_{osc}$ [GHz]	P [mW]	FOM
[3]	1.88-1.98	27	178
[4]	4.91-5.23	21	168
[5]	1.36-1.66	30	181
[11]	1.77-1.99	20	185
[6]	1.64-1.97	50	178
<b>This work</b>	<b>4.60-5.20</b>	<b>22</b>	<b>185</b>

## 6. Conclusion

A new quadrature-coupling concept has been introduced. In the proposed scheme, two oscillators are injection-locked in quadrature by means of common-mode inductive coupling. This gives quadrature over a wide tuning range, without introducing any phase noise- or power consumption increase. The advantages over conventional ring-based quadrature oscillators have been discussed. A  $0.25\mu\text{m}$ -CMOS  $5\text{GHz}$  quadrature VCO demonstrates the proposed concept, featuring a phase noise lower than  $-124\text{dBc/Hz}$  at  $1\text{MHz}$  offset over the  $4.6\text{-}5.2\text{GHz}$  tuning range at  $22\text{mW}$  power consumption.

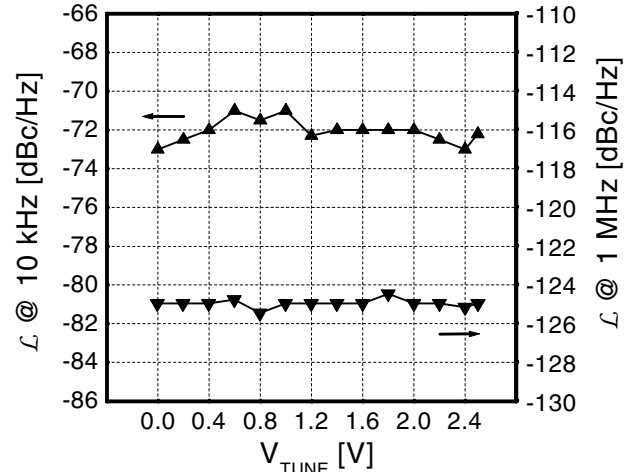


Figure 6. Measured phase noise over tuning range.

## 7. References

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